4/4 B.Tech. SEVENTH SEMESTER

EM7L1 ECAD LAB Credits: 2
Lecture: 3 periods/week Internal assessment: 25 marks
Tutorial: 0 period /week Semester end examination: 50 marks

Learning objective:

To familiarize the students verify the operations of the Digital IC's (hardware) and design and verify Digital IC's using software tool

Learning outcome:

Student will be able to :

- verifying the operation of Digital IC's based on its truth table
- Design combinational and sequential circuits in **VHDL** using XILInX and Simulate its functions Using **ISIM** Simulator tool

Simulate the Internal structure of the following Digital IC's using VHDL and verify the operations of the Digital IC's (Hardware) in the Laboratory :

1. 4-Bit Full adder -7483
2. 4-bit full subtractor-7483
3. D Flip-Flop 7474
4. Decade counter-7490
5. 4-bit counter -7493
6. shift registers-7495
7. 3-8 Decoder -74138
8. 4 bit Comparator-7485
9. 8 x 1 Multiplexer -74151 and 2x4 Demultiplexer-74155RAM (16x4)-74189 (Read and Write operations)
10. ALU Design